

**IN THE UNITED STATES PATENT AND TRADEMARK OFFICE**

<b>Applicants:</b>	Harold M. Chase, et al.	<b>Examiner:</b>	Unassigned
<b>Serial No.:</b>	To Be Assigned	<b>Art Unit:</b>	Unassigned
<b>Filed:</b>	Herewith	<b>Docket:</b>	12675Z
<b>For:</b>	METHOD FOR VLSI SYSTEM DEBUG AND TIMING ANALYSIS		<b>Dated:</b> September 16, 2003

Commissioner for Patents  
P.O. Box 1450  
Alexandria, VA 22313-1450

**PRELIMINARY AMENDMENT**

Sir:

Please amend the subject patent application as follows:

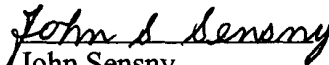
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Dated: September 16, 2003

  
John Sensny